

IN THE SPECIFICATION

Please amend the title to -HIGH-SPEED CLOCK AND DATA RECOVERY CIRCUIT-.

Please amend the paragraph at page 4, line 17 as follows:

FIG. 1A is a block diagram that illustrates the architecture of a clock and data recovery (CDR) circuit 10 according to the preferred embodiment of the present invention. The CDR circuit 10 includes: (1) a multi-phase voltage-controlled oscillator (VCO) 12 for accepting a control signal and for changing a frequency of a clock signal output from the VCO 12 in response thereto, wherein the VCO 12 outputs a plurality of phases of the clock signal; (2) a quarter-rate phase detector (PD) 14 for sampling an input data signal using the phases of the clock signal received from the VCO 12 and generating a plurality of data output data signals in response thereto, wherein each of the data output data signals detects an edge or transition in the input data signal and whether the edge is early or late with respect to its corresponding clock signal phase; (3) a Voltage-to-Current (V/I) Converter 16 for converting the data output data signals from the phase detector 14 to a control current; and (4) a loop filter (LPF) 18 for integrating the control voltage current from the V/I Converter 16 and for outputting the control signal to the VCO 12 in response thereto.

Please amend the paragraph at page 4, line 30 as follows:

Specifically, the circuit 10 accepts a single 40-Gb/s input data signal D_{in} , and re-times and de-multiplexes the input data signal D_{in} into a plurality of 10-Gb/s output data signals $D_{1_{out}}$, $D_{2_{out}}$, $D_{3_{out}}$ and $D_{4_{out}}$. To accomplish this function, the PD 14 uses half-quadrature phases of the clock signal CK provided by the VCO 12 to sample the input data signal D_{in} , thereby detecting the edges or transitions in the data input data signal D_{in} and determining whether the clock signal CK is early or late. Specifically, four 10-GHz phase offsets CK_0 , CK_{45} , CK_{90} and CK_{135} of the clock signal are output from the VCO 12, wherein adjacent ones of the phase offsets CK_0 , CK_{45} , CK_{90} and CK_{135} of the clock signal are half-quadrature phases, i.e., are offset in phase by 45° as indicated by their subscripts.

Please amend the paragraph at page 8, line 8 as follows:

FIG. 4A is a schematic of the master-slave flip-flop 20 used in the PD 14 according to the preferred embodiment of the present invention. The master-slave flip-flop 20 includes switches M_1 , M_{13} and M_4 and capacitors C_1 - C_2 . The flip-flop 20 latches input data signal D_{in} , using a CK clock signal provided from the VCO 12 buffer, and data output data signals D_{out} .